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DC/DC Switching Power Converter with Digital Control based on FPGA

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Abstract

The paper first deals with the design of a DC/DC switching boost converter with digital control based on FPGAs, which is suitable for space applications. Digital control systems have significantly advantages over conventional pulse width modulator (PWM) controllers. Indeed, along with the general advantages of a digital system, such as reduced sensitivity to noise and component parameter variations, and the capability to realize sophisticated control algorithms, a digital controller can be hardened more easily against radiation-induced errors than its analog counterpart. Besides, the implementation of the digital controller in a SRAM FPGAs provides more flexibility in terms of quick turn-around time, and on-orbit reconfiguration capability. However, SRAM-based FPGAs are very sensitive to single-event effects (SEEs). Therefore, we propose a radiation-hardness-by-design (RHBD) technique based on logic duplication approach at both logic and device levels and on non-disruptive resynchronization mechanism that ensures the continuous operation of the converter when facing the issue of single-event functional interrupts (SEFIs) that may occur in SRAM-based FPGAs. This technique is validated with both VHDL simulations and experimental results.

Keywords: radiation-hardness-by-design, FPGAs, pulse width modulator, switching, DC/DC boost converter

INTRODUCTION

DC/DC switching power converters, due to their high-efficiency conversion, are essential parts of the power conditioning system of a satellite [1]. The aim of this work is the design of a radiation hardened FPGA-based digital control system for a boost converter. Digital control systems have significant advantages over conventional analog pulse width modulators (PWMs). The use of commercial SRAM-based FPGAs in space applications is very attractive because of their high component density, quick turn-around time, and reconfigurability. However, SRAM-based FPGAs are very sensitive to SEEs. Indeed, along with the general advantages of a digital system (such as high flexibility, reduced sensitivity to noise and component parameter variations, and the capability to realize sophisticated control algorithms [2]), a digital controller can be hardened more easily against radiation-induced errors than its analog counterpart. In fact, a conventional PWM switching converter is very susceptible to single-event effects (SEEs) in the error amplifier stage and in the analog PWM controller that cause large transient pulses at its output [3], [4].

The dominant effect is the single event functional interrupt (SEFI) caused to a configuration memory bit upset that disrupts the continuous operation of the system in which the FPGA is used. Heavy ion testing on these devices has shown that no permanent faults occur after a SEFI, and that reprogramming the FPGA will restore full functionality [5]. Therefore, “radiation hardening by design” (RHBD) techniques based on detecting, mitigating and correcting SEFIs make it possible to use SRAM-based FPGAs in space applications.

DESIGN AND RESULTS

Fig 4.a shows the basic structure of a digitally controlled DC/DC switching boost converter. The actual output voltage $v(t)$ is divided by the sensor gain (H) and converted into a digital signal $v_q[n]$ by means of a sampling process and analog-to-digital conversion (ADC). The difference between the digitized sample of the converter output and the reference voltage (N_{ref}) forms an error signal $e[n]$ that is processed by the digital regulator to calculate the actual duty cycle $d[n]$. Eventually, the digital pulse width modulator (DPWM) generates the switching signal $d(t)$ that controls the power MOSFET. In our design, we apply the 1-bit error resolution technique that uses a deadzone comparator to perform the A/D conversion and a simple up/down counter to calculate the duty cycle [7].

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To implement the digital controller in an SRAM-based FPGA, we apply a RHBD technique that mitigates and corrects SEFIs. When applying a digital control using an SRAM-based FPGA in a switching converter application, radiation induced SEFIs result in missing pulses in the generated PWM control signal of the converter. In turn, the missing pulses result in large transient voltage drops at the output of the converter that may adversely affect the operation of the powered systems [3], [4]. As a result, a redundant approach at both the logic design and the device levels has been applied.

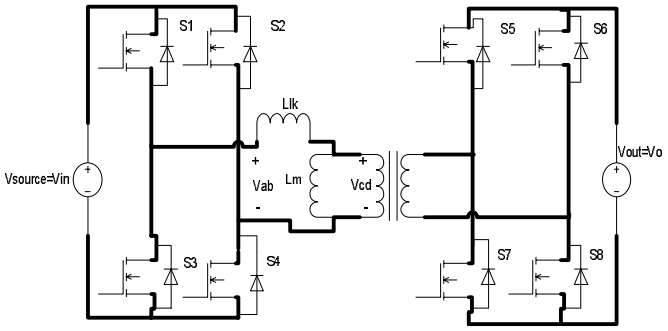

Fig. 1 – Full bridge DC/DC converter

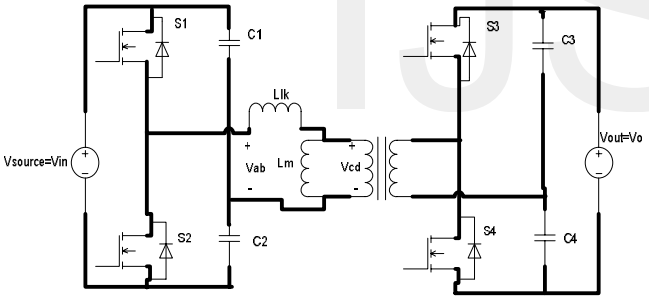

Fig. 2 – Half bridge DC/DC converter

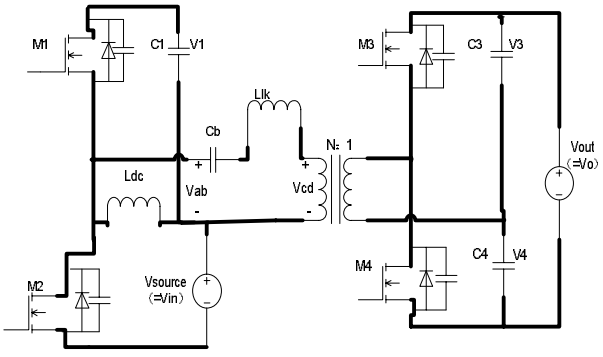

Fig. 3 – New half bridge DC/DC converter

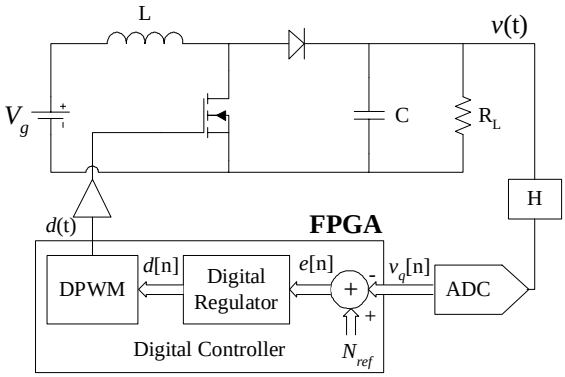

Fig.4. Basic schematic of a digitally controlled boost converter

As shown in Fig. 1.b, the outputs of two identical logic blocks inside each FPGA are continuously compared to each other using an XNOR gate. An error in either logic block due to a SEU in a user register or a SEFI in the related configuration bits will deactivate the tri-state output buffers of the FPGA. Consequently, the failed device goes in an offline status in which all its outputs are in a high impedance state. A temporary data upset due to an SEU in a user register will quickly disappear, and the two logic blocks will resynchronize. However, a configuration bit SEFI will result in continuous disagreement between the two logic blocks. The remaining FPGA continues to generate the correct outputs, so that the continuous operation of the overall system is guaranteed.

The recovery from an error condition due to a SEFI is achieved by a cross-checking procedure. Each FPGA continuously monitors the operating state of the other FPGA. If an incorrect operating condition is detected, the failed device is reconfigured. The SEFI detection can be performed by reading back the actual configuration data and comparing it with the original configuration bit-stream. However, this approach relies on a particular feature available only on Vertex FPGAs [6]. A more general approach was applied based on the detection of the offline status of an FPGA through the use of a watchdog counter. The expiring counting value can be set so that an error due to a temporary upset, such as a user register flip, does not force the reconfiguration of the FPGA.

Unfortunately, a reconfiguration alone is not sufficient to restore the system to full functionality because the two FPGAs must resynchronize their current operating states. The simplest way to achieve this is by means of a general reset. However, a reset will disrupt the current state of the system, and an undesirable transient pulse will result at the DC/DC converter output. To avoid this transient error, the logic block was designed so that the reconfigured device can load the current state of the system from the device that is still operating.

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In order to validate this approach a proof-of-concept demonstration was implemented using Altera FPGAs from the FLEX10K family. An error injection block is used to simulate the occurrence of an error into a logic block, and a reconfiguration emulator block is used to emulate the reconfiguration phase. The reconfiguration emulator module forces the output of the related device to a high impedance state during the configuration period, and at its end forces a reset of the device. Fig. 1.a shows the VHDL simulation of the overall system. Note that after the injection of an error in the first FPGA, the second FPGA detects the incorrect status of the first device through the offline signal and forces its reconfiguration. During the reconfiguration and the resynchronization phases, the second device generates the correct PWM waveform, and at the end of those phases the reconfigured device restarts operation with the correct duty cycle.

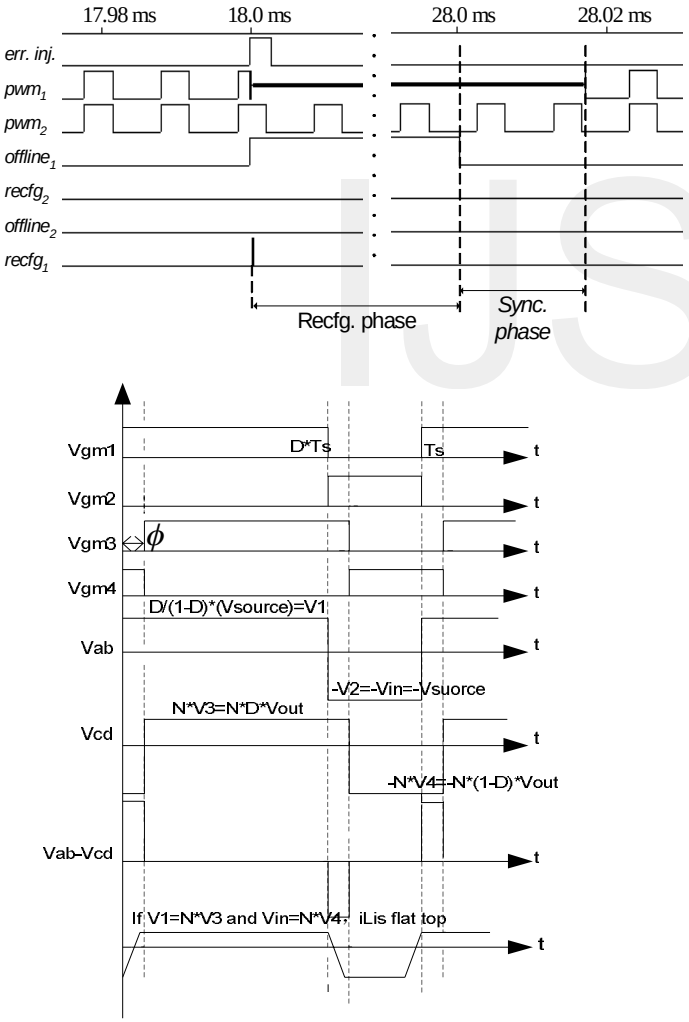

Fig. 1. simulation of the overall system

CONCLUSION

This work demonstrates the design of a digitally controlled boost converter suitable for space applications based on an SRAM FPGA. A RHBD technique has been developed and applied to assure the continuous operation of the converter in the presence of SEEs (more precisely SEFIs) that can occur in the FPGA device. This technique utililizes redundant logic combined with a non-disruptive procedure to resynchronize the two devices after a reconfiguration. The proposed approach has successfully been validated through both VHDL simulations and experiments performed on a proof-of-concept demonstrator constructed using off-the-shelf FPGA devices.

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